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| EXAMINER | |
|---|---|
| PROCTOR, JASON SCOTT | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/707,448 | PIPPIN, JACK D. | |
| | Examiner | Art Unit | |
| | JASON PROCTOR | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *3-11 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-11 and 13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/8/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

Claims 3-11 and 13-21 were rejected in the Office Action entered on 6 March 2008.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 September 2008 has been entered.

The 8 September 2008 submission comprised a request for reconsideration.

Claims 3-11 and 13-21 are pending in this application.

Claims 3-11 and 13-21 are rejected.

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on 8 September 2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

In that IDS, the citation for reference CL cites 178 pages. Only 125 pages have been received. Also, references CAA, CHH, and CII have not been found. These citations have been lined through and the references have not been considered.

The citation of reference CJJ has been corrected by the Examiner to include the date found on the first page of that reference.

***Response to Arguments – 35 USC § 103***

2. In response to the previous rejections under 35 U.S.C. § 103 based upon Kenny, Farwell, and Emery, Applicants argue primarily that none of the references disclose a plurality of thermal sensors placed at different locations on an integrated circuit nor sensing temperature at a plurality of different locations on an integrated circuit, as recited by the independent claims.

The Examiner has fully considered this argument and finds it persuasive in combination with the remainder of Applicants' remarks. Accordingly, the previous rejections have been withdrawn. New grounds of rejection have been entered below.

The Kenny reference is relied upon in the new grounds of rejection entered below. Applicants' remarks regarding the Kenny reference have been fully considered, but would not overcome the new rejections. In those remarks, Applicants refer to the previous Office Action as conceding that Kenny does not expressly suggest "an averaging mechanism as recited by the claims." (Remarks, page 5) Upon further consideration of the Kenny reference, Kenny does teach an averaging mechanism [*"The 'hot' and 'cool' samplings are averaged through an up/down counter."* (column 2, lines 2-17)].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 3-5, 8, 13-15, and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 3,383,614 to Emmons et al. ("Emmons") in view of US Patent No. 5,287,292 to Kenny et al. ("Kenny").

Regarding claim 3, Emmons teaches:

An integrated circuit comprising [*"This invention relates to temperature stabilized semiconductor devices..."* (column 1, lines 20-30)]:

A plurality of thermal sensors each placed in one of a plurality of different locations on the integrated circuit [*"In accordance with a preferred embodiment of this invention, this is accomplished by fabricating the substrate, its insulation from the ambient, and the components on the substrate in such a manner as to establish a controlled temperature gradient pattern over the substrate as a result of the introduction of heat to the substrate by a heater located on the substrate.* ***A plurality of sensors are positioned at the other end of the substrate and arrayed*** *so as to determine the effective center of sensing within a control region..."* (column 2, lines 10-30)];

An averaging mechanism to calculate an average temperature from the plurality of sensors [*"**The sensors and heater** are part of an electrical amplifier which produces a negative thermal feedback **and maintains the average temperature of the control region within a given temperature range**"* (column 2, lines 10-30); See sensors D1-D14 in FIG. 1; *"**All of the other sensing elements, i.e., the diodes D1-D14**, are disposed at the opposite end of the substrate 10. It will be noted that the diodes D1-D14 are also disposed symmetrically about the axis 60 and **are also spaced transversely from and extend longitudinally of the axis 60 so as to sample the temperature of the substrate** around the control region 25. The transistors Q1 and Q2, which also act as sensors to a small degree, are located on the axis 60."* (column 4, line 47 - column 5, line 5)].

Emmons does not teach a register associated with the averaging mechanism as claimed.

Kenny teaches a CPU integrated circuit with a heat regulator circuit on the same integrated circuit as the CPU, including a register associated with the averaging mechanism to store a threshold temperature value and interrupt logic associated with the averaging mechanism to generate an interrupt if the calculated average temperature exceeds the threshold temperature. [*"'Hot' and 'cold' readings are **averaged through an up/down counter**. If the counter increments (i.e. measures the CPU speed to be 'hot') more than it decrements (i.e. measures the CPU speed to be 'cool'), **the count will eventually reach a threshold value that will trigger regulation of the CPU speed**. Whenever the threshold is reached, the CPU clock speed is slowed."* (column 2, lines 2-18)]. The Examiner submits that a "counter" necessarily involves a

register, and a CPU that "triggers regulation of the CPU speed" necessarily involves interrupt logic to generate an interrupt.

Emmons and Kenny are analogous art because both are directed to thermal control of integrated circuits.

Kenny expressly provides motivation to combine the teachings, such as to ensure the safe operation of a circuit that has reached its "thermal equilibrium" [*"An integrated circuit operating at a constant fixed level of activity has an equilibrium temperature which is eventually reached. At equilibrium, the heat lost to the surroundings of the circuit on average equals the heat generated by the circuit. The temperature therefore remains roughly constant. Unfortunately, the equilibrium temperature of an integrated circuit is often above the safe operating temperature and a cooling scheme is needed."* (Kenny, column 1, lines 10-18)]. By combining this feature with the teachings of Emmons, a "temperature stabilized semiconductor device" having a plurality of sensors and an averaging mechanism is improved by slowing CPU speed to prevent excessively hot and unsafe operating temperatures.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Emmons and Kenny to arrive at the invention specified in claim 3.

Regarding claim 4, see Kenny, column 2, lines 2-18 (shown above).

Regarding claim 5, Kenny teaches that the register is programmable by the integrated circuit [*"The circuit is forced to cool if a count on the up/down counter reaches a programmable threshold."* (abstract)].

Regarding claim 8, Kenny teaches clock adjustment logic to control the temperature of the integrated circuit by increasing and decreasing an integrated circuit clock frequency in response to the calculated average temperature [*" 'Hot' and 'cold' readings are averaged through an up/down counter. If the counter increments (i.e. measures the CPU speed to be 'hot') more than it decrements (i.e. measures the CPU speed to be 'cool'), the count will eventually reach a threshold value that will trigger regulation of the CPU speed.* ***Whenever the threshold is reached, the CPU clock speed is slowed."*** (column 2, lines 2-18)].

Regarding claim 13, Kenny teaches comparing each of the plurality of sensed temperatures to a threshold and generating an interrupt in response thereto (column 2, lines 2-18).

Regarding claim 14, Emmons teaches a sensing temperature at a plurality of different locations on an integrated circuit [*"In accordance with a preferred embodiment of this invention, this is accomplished by fabricating the substrate, its insulation from the ambient, and the components on the substrate in such a manner as to establish a controlled temperature gradient pattern over the substrate as a result of the introduction of heat to the substrate by a heater located on the substrate.* ***A plurality of sensors are positioned at the other end of the substrate***

***and arrayed*** *so as to determine the effective center of sensing within a control region..."* (column 2, lines 10-30)]; and

Calculating an average temperature from the plurality of different sensed temperatures [*"**The sensors and heater** are part of an electrical amplifier which produces a negative thermal feedback **and maintains the average temperature of the control region within a given temperature range**"* (column 2, lines 10-30); See sensors D1-D14 in FIG. 1; *"**All of the other sensing elements, i.e., the diodes D1-D14**, are disposed at the opposite end of the substrate 10. It will be noted that the diodes D1-D14 are also disposed symmetrically about the axis 60 and **are also spaced transversely from and extend longitudinally of the axis 60 so as to sample the temperature of the substrate** around the control region 25. The transistors Q1 and Q2, which also act as sensors to a small degree, are located on the axis 60."* (column 4, line 47 - column 5, line 5)].

Kenny teaches storing a threshold temperature value in a register and generating an interrupt if the calculated average temperature exceeds the stored threshold temperature [*" 'Hot' and 'cold' readings are **averaged through an up/down counter**. If the counter increments (i.e. measures the CPU speed to be 'hot') more than it decrements (i.e. measures the CPU speed to be 'cool'), **the count will eventually reach a threshold value that will trigger regulation of the CPU speed**. Whenever the threshold is reached, the CPU clock speed is slowed."* (column 2, lines 2-18)]. The Examiner submits that a "counter" necessarily involves a register, and a CPU that "triggers regulation of the CPU speed" necessarily involves interrupt logic to generate an interrupt.

Regarding claim 15, Kenny teaches decreasing a clock frequency of the integrated circuit in response to an interrupt indicating that the threshold temperature has been exceeded [*"... During this time* [when the CPU is hot] *the counter increments once each timing cycle and reaches the threshold of 8. The CPU is forced to low speed for a timing cycle, and the counter decrements to 7."* (column 6, line 62 – column 7, line 11)].

Regarding claim 18, Kenny teaches controlling the temperature of the integrated circuit by increasing and decreasing an integrated circuit clock frequency in response to the calculated average temperature [*" 'Hot' and 'cold' readings are averaged through an up/down counter. If the counter increments (i.e. measures the CPU speed to be 'hot') more than it decrements (i.e. measures the CPU speed to be 'cool'), the count will eventually reach a threshold value that will trigger regulation of the CPU speed.* ***Whenever the threshold is reached, the CPU clock speed is slowed."*** (column 2, lines 2-18)].

4. Claims 6-7, 9, 16-17, 19, and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Emmons in view of Kenny as applied to claims 3, 5, and 14 above, and further in view of US Patent No. 5,255,149 to Matsuo.

Regarding claims 6 and 7, Emmons in view of Kenny does not explicitly teach the claimed "threshold adjustment logic".

Matsuo teaches threshold adjustment logic to program the register to a different threshold temperature in response to an interrupt from the interrupt logic indicating that the threshold temperature has been exceeded [See FIG. 3, S102, S105, S108, S109; also *"a temperature abnormality detector for an electronic apparatus, comprising a plurality of temperature sensors arranged near a heat-generating electronic part mounted on an electronic apparatus,* [...] *second discriminating means for determining whether* ***the measured temperature value reaches a first level set within the predetermined range and a second level set as a value larger than that of the first level...***" (column 2, lines 40-65)].

Emmons in view of Kenny and Matsuo are analogous art because both are directed to thermal control of integrated circuits.

Matsuo expressly provides motivation to combine the teachings, such as to detect and recover from a failure in one of a plurality of thermal sensors [*"It is still another object of the present invention to provide a temperature abnormality detector for an electronic apparatus, capable of discriminating a sensor failure from a temperature abnormality to repair and restore the apparatus for a short time."* (Matsuo, column 2, lines 35-40). By combining this feature with Emmons in view of Kenny, a "temperature stabilized semiconductor device" having a plurality of sensors and an averaging mechanism, and having CPU clock speed slowdown to prevent overheating, would be even more reliable because of Matsuo's method of detecting a sensor failure.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Emmons in view of Kenny and Matsuo to arrive at the invention specified in claims 6 and 7.

Regarding claim 9, Matsuo teaches halt logic to halt operation of the integrated circuit in response to the calculated average temperature [*"**halt means** for interrupting power supply to the electronic part and halting the electronic apparatus when the measured temperature value reaches the first level and then the second level on the basis of an output from the second discriminating means."* (column 2, lines 60-68)].

Regarding claims 16-17, Matsuo teaches programming the register to a second different threshold temperature in response to an interrupt indicating that the threshold temperature has been exceeded [See FIG. 3, S102, S105, S108, S109; also *"a temperature abnormality detector for an electronic apparatus, comprising a plurality of temperature sensors arranged near a heat-generating electronic part mounted on an electronic apparatus,* [...] *second discriminating means for determining whether* ***the measured temperature value reaches a first level set within the predetermined range and a second level set as a value larger than that of the first level...***" (column 2, lines 40-65)].

Regarding claim 19, Matsuo teaches halting operating of the integrated circuit in response to the calculated average temperature [*"**halt means** for interrupting power supply to the electronic part and halting the electronic apparatus when the measured temperature value*

*reaches the first level and then the second level on the basis of an output from the second discriminating means."* (column 2, lines 60-68)].

Regarding claim 21, Matsuo teaches generating a first interrupt if the calculated average temperature exceeds a first threshold and a second interrupt if the calculated average temperature exceeds a second threshold (column 2, lines 40-68).

5. Claims 10 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Emmons in view of Kenny, further in view of US Patent No. 3,843,872 to Shimomura.

Regarding claim 10, the rationale shown in the rejection of claim 1 is incorporated. Emmons in view of Kenny teaches an integrated circuit comprising a plurality of thermal sensors and an averaging mechanism as recited by claim 10. Emmons in view of Kenny does not expressly teach an interrupt handler as claimed.

Shimomura teaches an integrated circuit for precision temperature measurement comprising a resistor or thermocouple as a temperature sensor (abstract). Temperature measurements are taken and a computation is performed on those measurements, producing an output result stored in a counter [See column 3, lines 45-50; the function is described in columns 4-5, resulting in ["*For example, of n=100, the contents of the counter 2 may be converted through a binary-to-decimal converter 33 under the control of a controller 32 into a corresponding decimal number, which may be displayed at an indicator 34, and whose 1/100*

*fraction may be read. Numeral 35 designated a clear terminal of the controller 32."* (column 6, lines 23-30)]. Shimomura therefore teaches an interrupt handler to display information regarding the calculated average temperature to a user of the integrated circuit.

Emmons in view of Kenny and Shimomura are analogous art because both are directed to thermal control of integrated circuits.

Shimomura expressly provides motivation to combine the teachings, such as to achieve extremely high precision and to provide correction in temperature and other measurements (column 2, lines 15-24). By combining this feature with Emmons in view of Kenny, an integrated circuit having a plurality of sensors and an averaging mechanism, and having CPU clock speed slowdown to prevent overheating, benefit from reliable, high precision temperature readings.

Claim 20 recites a method corresponding to the integrated circuit of claim 10. For rationale similar to that shown above regarding claim 10, Emmons in view of Kenny, further in view of Shimomura teaches the invention of claim 20.

6. Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Emmons in view of Kenny, further in view of Shimomura as applied to claim 10, further in view of Matsuo.

Regarding claim 11, Emmons in view of Kenny, further in view of Shimomura fails to expressly teach the interrupt logic recited by claim 11.

Matsuo teaches interrupt logic to generate a first interrupt if the calculated average temperature exceeds a first threshold and a second interrupt if the calculated average temperature exceeds a second threshold [See FIG. 3, S102, S105, S108, S109; also *"a temperature abnormality detector for an electronic apparatus, comprising a plurality of temperature sensors arranged near a heat-generating electronic part mounted on an electronic apparatus,* [...] *second discriminating means for determining whether* ***the measured temperature value reaches a first level set within the predetermined range and a second level set as a value larger than that of the first level...***" (column 2, lines 40-65)].

Emmons in view of Kenny, further in view of Shimomura and Matsuo are analogous art because both are directed to thermal control of integrated circuits.

Matsuo expressly provides motivation to combine the teachings, such as to detect and recover from a failure in one of a plurality of thermal sensors [*"It is still another object of the present invention to provide a temperature abnormality detector for an electronic apparatus, capable of discriminating a sensor failure from a temperature abnormality to repair and restore the apparatus for a short time."* (Matsuo, column 2, lines 35-40). By combining this feature with Emmons in view of Kenny, further in view of Shimomura, a "temperature stabilized semiconductor device" having a plurality of sensors and a highly precise averaging mechanism, and having CPU clock speed slowdown to prevent overheating, would be even more reliable because of Matsuo's method of detecting a sensor failure.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Emmons in view of Kenny and Matsuo to arrive at the invention specified in claim 11.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jason Proctor/
Examiner
Art Unit 2123

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